TRANSFER MODE; U.S. Patent Application No. 09/964,315 TI-31779); filed on even data herewith; invented by Shakuntala Anjanaiah and Natarajan Seshan; and assigned to the assignee of the present application: APPARATUS AND METHOD FOR AN INTERFACE UNIT FOR DATA TRANSFER BETWEEN A HOST PROCESSING AND A MULTI-TARGET DIGITAL SIGNAL PROCESSING IN AN ASYNCHRONOUS TRANSFER MODE; U.S. Patent Application No. 09/964,158; filed on even date herewith; invented by Martin Li, Jay Reimer Shakuntala Anjanaiah, Natarajan Seshan and Patrick Smith; and assigned to the assignee of the present application: and APPARATUS AND METHOD FOR INPUT CLOCK SIGNAL DETECTION IN AN ASYNCHRONOUS TRANSFER MODE INTERFACE UNIT; U.S. Patent Application No. (Attorney Docket No. 09/964,164; filed on even date herewith; invented by Shakuntala Anjanaiah; and assigned to the assignee of the present application are related applications.

Please delete the Paragraph beginning on page 3, line 4 and replace this Paragraph with the following Paragraph.

"The asynchronous transfer mode interface unit is only one of the possible devices that can provide an interface between a digital signal processing unit and other data processing devices. Another interface device is the I/O interface device. In fabricating a chip, the device can include one type of interface unit or both types of interface units. The inclusion of only one type of interface unit limits the utility of the chip. The inclusion of both types of interface units on a chip

increases ~~the~~ both the size and the complexity of the chip."

Please delete the Paragraph beginning on page 13, line 30 and replace this Paragraph with the following Paragraph.

"Referring to Fig. 13, the operation of the (transmit) EVENT signal is illustrated. After initialization of the transmit portion of the UTOPIA interface unit in step 1300 or as part of the continuing operation of the interface unit, a determination is made in step 1301 whether a space for the storage of a complete data cell is available in the transmit buffer memory unit. When the determination is yes, then in step 1302 a transmit EVENT signal is applied to the direct memory access unit. In response to the generation of the EVENT signal, a data cell is transmitted through the direct memory access unit to the buffer memory storage unit in step 1303. In step 1304, as soon as the transfer of the data cell has begun and the first word of the cell is written, the EVENT signal is cleared. Note that the EVENT signal is reasserted as soon as the first word is written and the buffer memory unit has space available. The immediate assertion of the EVENT signal improves the interface unit throughput. The process ~~than returned~~ then returns to step 1301 to determine whether space in the transmit buffer memory unit is available for storage of an entire data cell. When the determination ~~is~~ in step 1301 is negative, the process returns to step 1301 and continues to cycle until space is available for the storage of an entire data cell.

Please delete the Paragraph beginning on page 16, line 21 and replace this Paragraph with the following Paragraph.

"The foregoing description has described the interface unit as including a buffer memory unit. In the preferred embodiment, the buffer memory unit is implemented by a first-in/first-out memory unit. The memory unit is pro9vided with the capacity to store two data cells. The communication bus causes the signals to be exchanged between the master unit and the slave unit to have a relatively slow clock speed. Because of the relatively slow clock speed of the communication bus, the filling or emptying of the buffer memory in the direction of the communication will be much slower than the filling and the emptying of the buffer memory unit in the directio0n of the direct memory access unit. Similarly, although the direct memory access unit can handle only one data transfer at a time, because of the difference in clock speed between the communication bus and the processing unit of which the direct memory access unit is ~~part~~ accommodated by the interface unit.

In the Claims

Please amend Claim 1 as follows.

1. (Currently Amended) An interface unit controlling the exchange of signals between a data processing unit and a communication bus, the data processing unit including a